LABORATORIO DI VISIONE ARTIFICIALE
Tel. 0382/391372 Telefax 0382/412881

Tecniche e Strumenti per l'Elaborazione di Immagini ed il Riconoscimento di Forme

Parte II: Livello Alto e Strumenti Disponibili

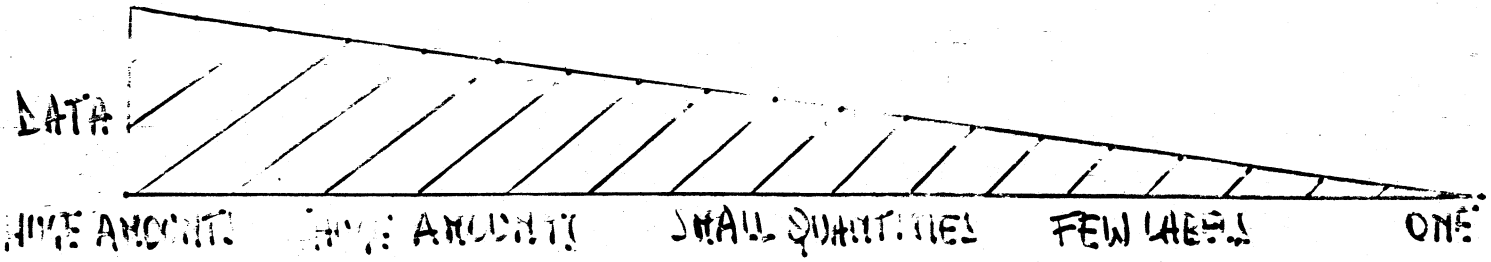
10. 1 Dicembre 1989
c/o SPERONI Spa, Spessa Po

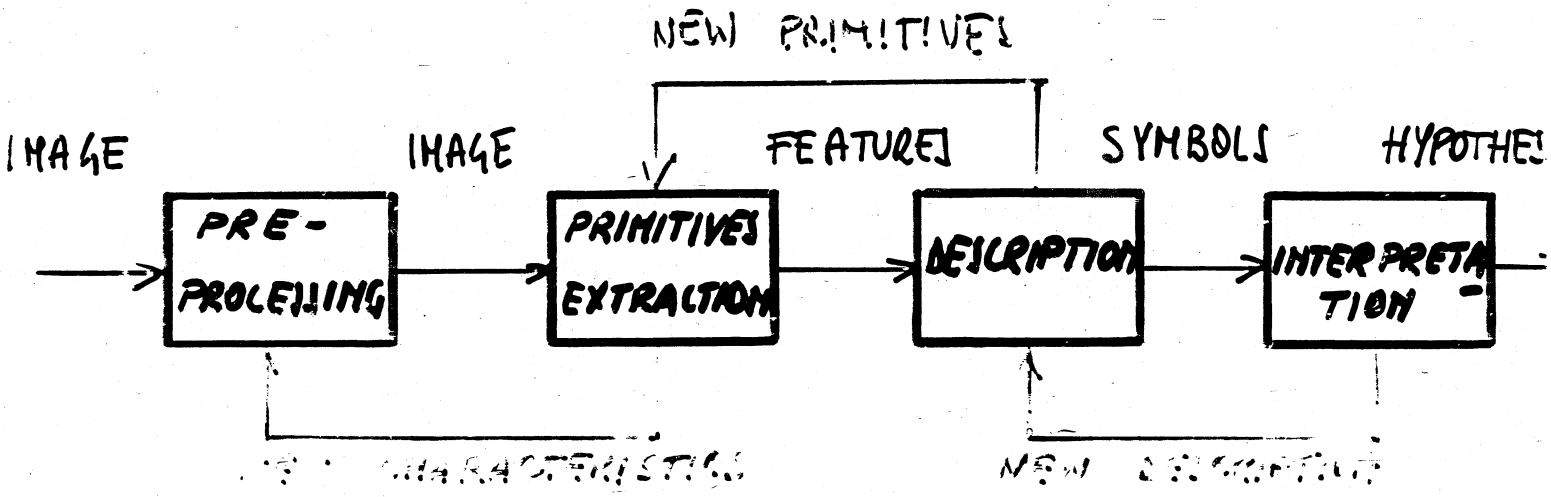
V. Cantoni:

Architetture e Linguaggi
per l'Elaborazione di Immagini
Reti Neurali.

Dipartimento di Informatica e Sistemistica, Università degli Studi di Pavia

IMAGE UNDERSTANDING PROCESS





HIERARCHICAL APPROACH

PREPROCESSING : Enhancement, restoration and preparation in view of an automatic design.
(point dependent, local, global)

PRIMITIVES EXTRACTION : Extraction of salient features and pertinent primitives.

SYMBOLIC DESCRIPTION : Compact description to make obvious relations among primitives.

INTERPRETATION : Understand the image content.

TIPO DI ELABORAZIONE / ARCHITETTURA

LIVELLO:

ELABORAZIONE A BASSO LIVELLO	ELABORAZIONE AD ALTO LIVELLO

DATI:

STRUTTURA REGOLARE	STRUTTURA NON REGOLARE
GRANDI QUANTITÀ	QUANTITÀ NON ELEVATE

PARALLELISMO:

BIT	SOTTO-PROGRAMMA
ACCESSO AI VICINI	
IMMAGINE	
OPERAZIONE	

ARCHITETTURA:

A MATRICE DI PROCESSORI "PIPELINE"	MULTIPROCESSORI A BUS
	ARCHITETTURE RICONFIGURABILI

IMAGE PROCESSING ARCHITECTURES
CLASSIFICATION SCHEMES

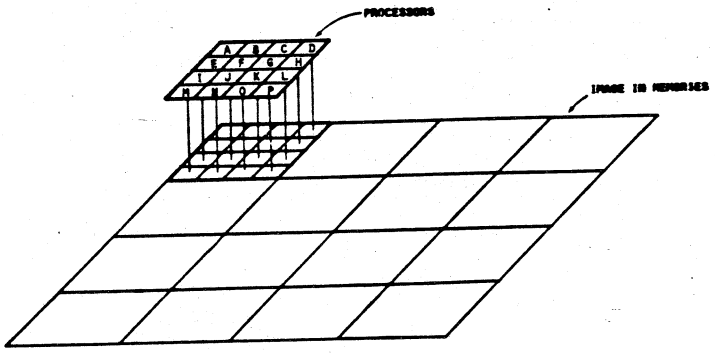
LEVELS OF PARALLELISM

Duff, Levialdi 1980

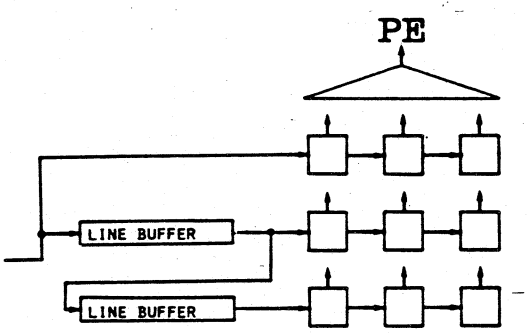
FOUR DIMENSIONS OF PARALLELISM MAY BE INTRODUCED:

- THE SEQUENCE OF OPERATIONS
  OPERATOR PARALLELISM = PIPELINING
- THE IMAGE COORDINATES
  IMAGE PARALLELISM
- THE NEIGHBORHOOD POINTS
  NEIGHBORHOOD PARALLELISM
- THE PIXEL BITS
  WORD CONVENTIONAL PARALLELISM

b1)



c)



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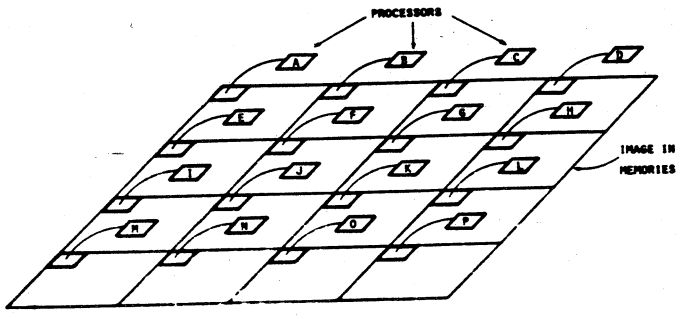


a)

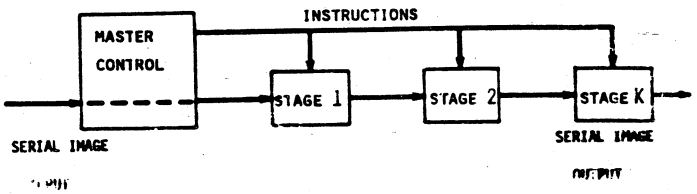
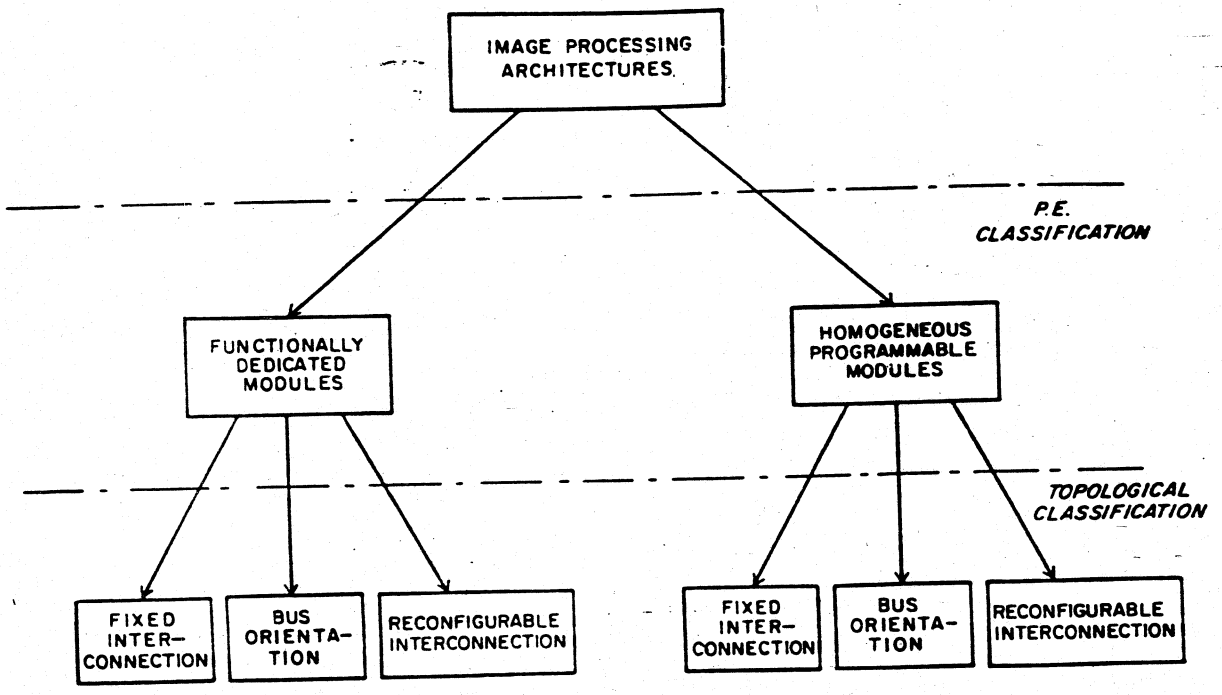


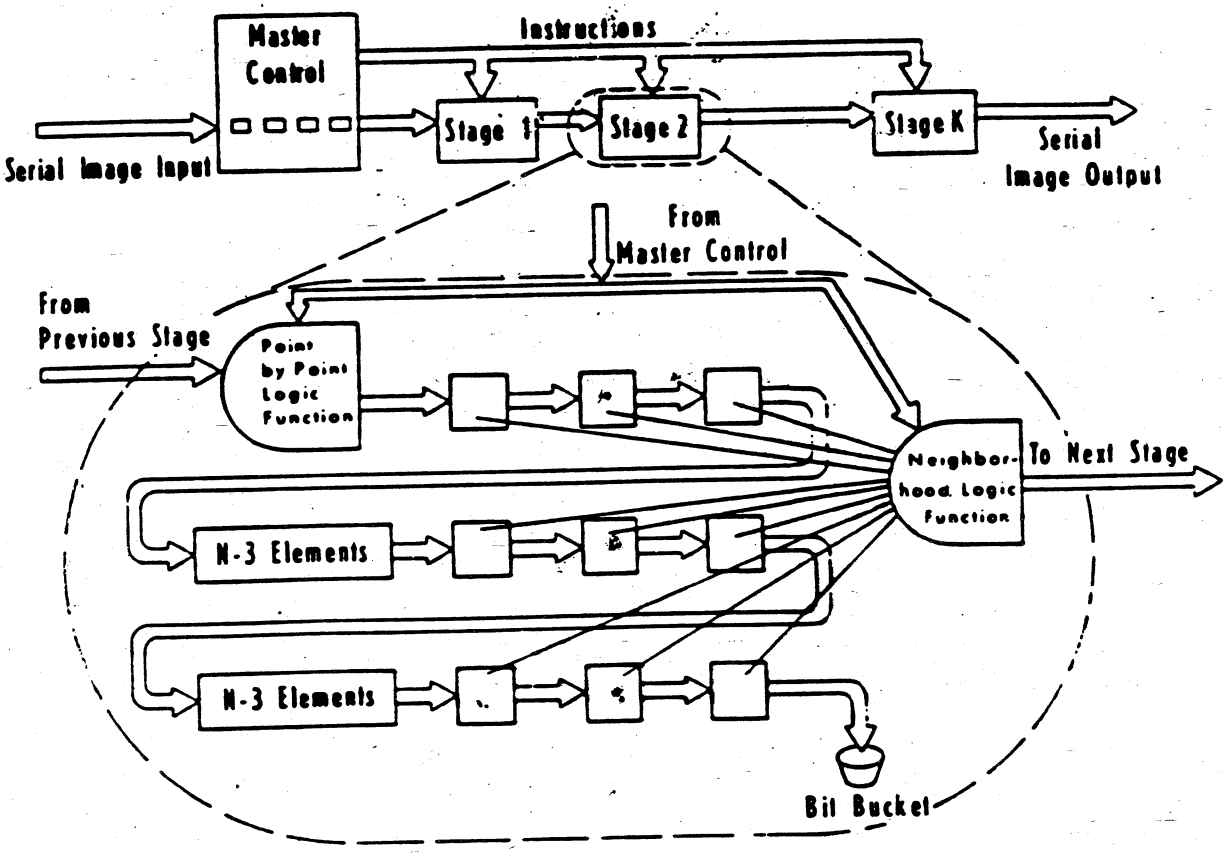
IMAGE PROCESSING ARCHITECTURES CLASSIFICATION SCHEMES

INTERPROCESSOR COMMUNICATION MODES

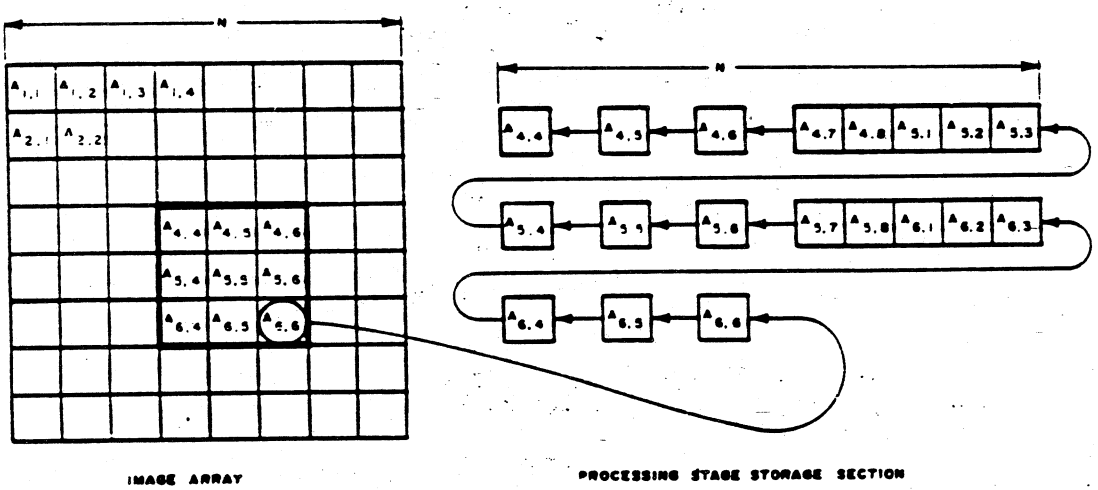


INTERPROCESSOR COMMUNICATION MODES

HETEROGENEOUS FUNCTIONALLY DEDICATED/FIXED INTERCONNECTED STRUCTURE



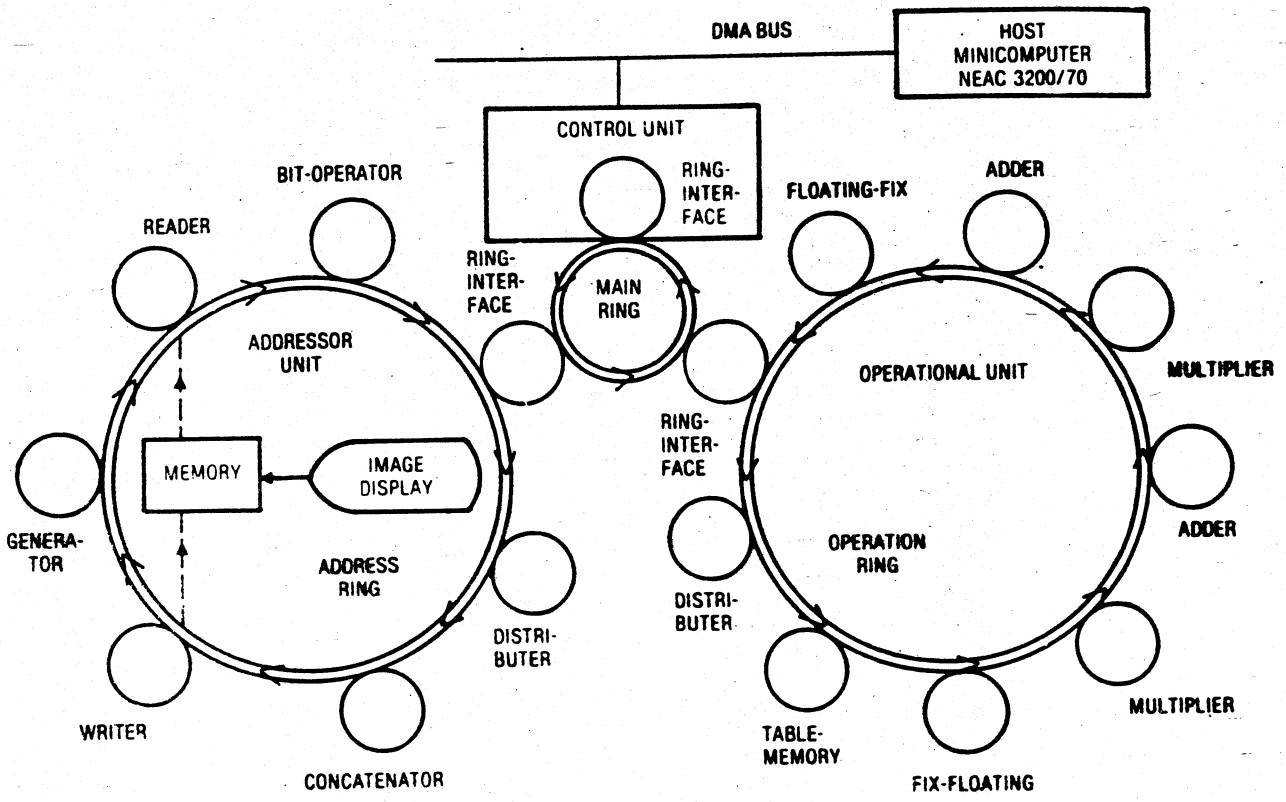
CYTOCOMPUTER



SYSTOLIC

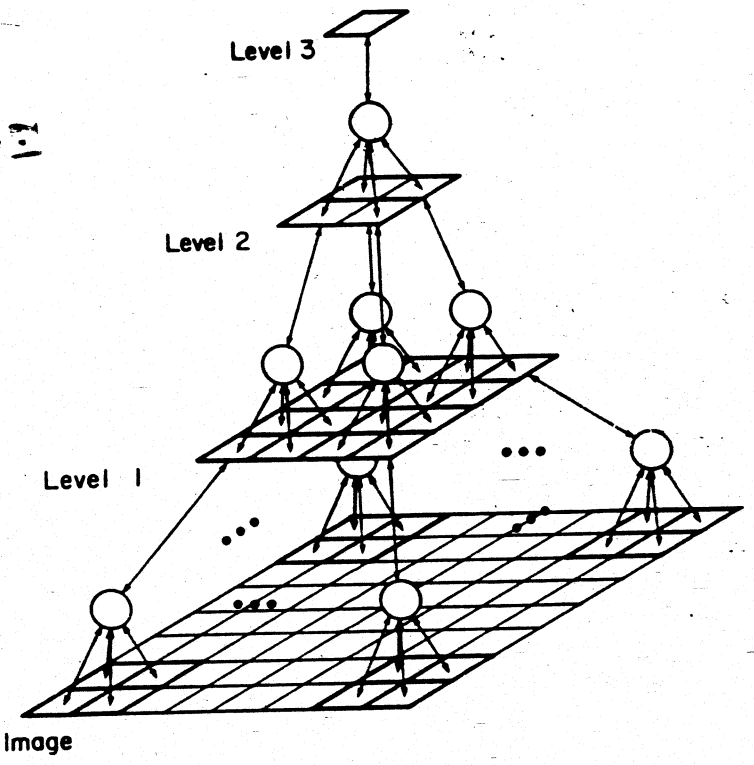
DATA DEPENDENT SYSTEMS

DATAFLOW ARCHITECTURE FOR IMAGE PROCESSING



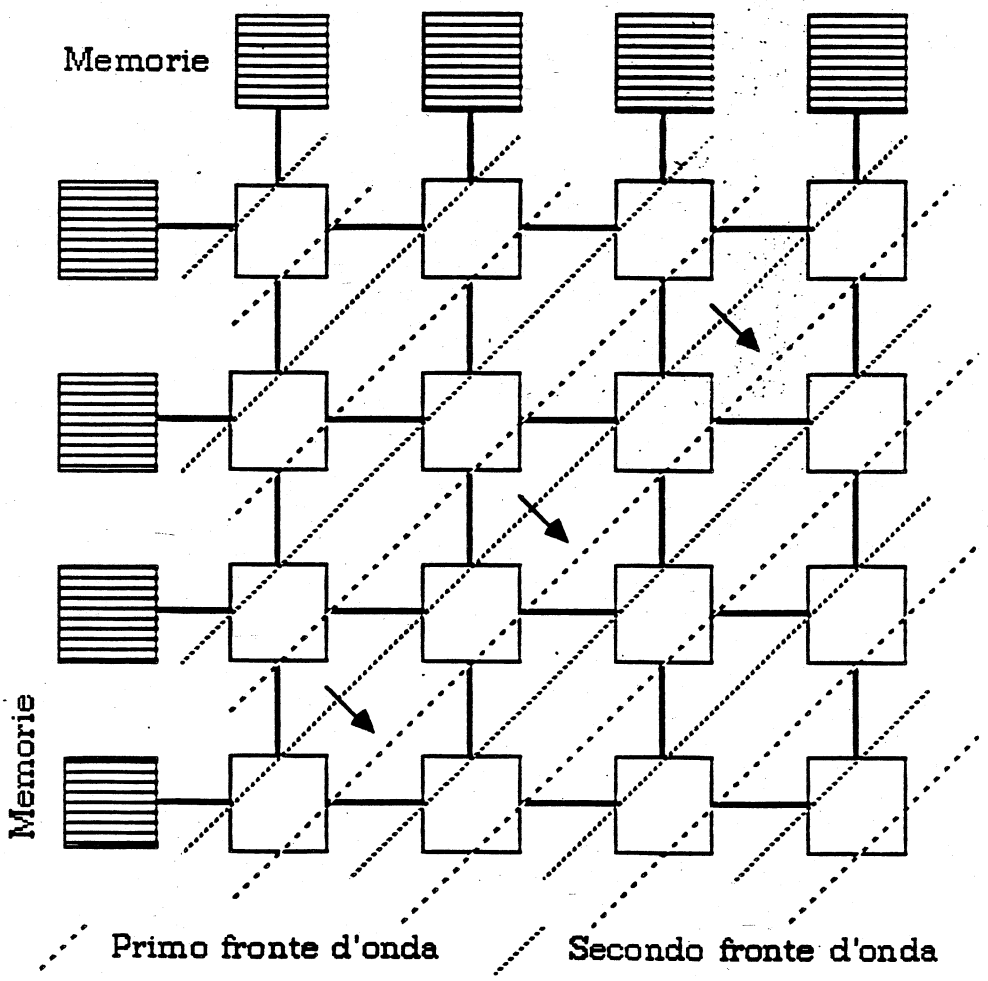
TIP

PIRAMID STRUCTURE

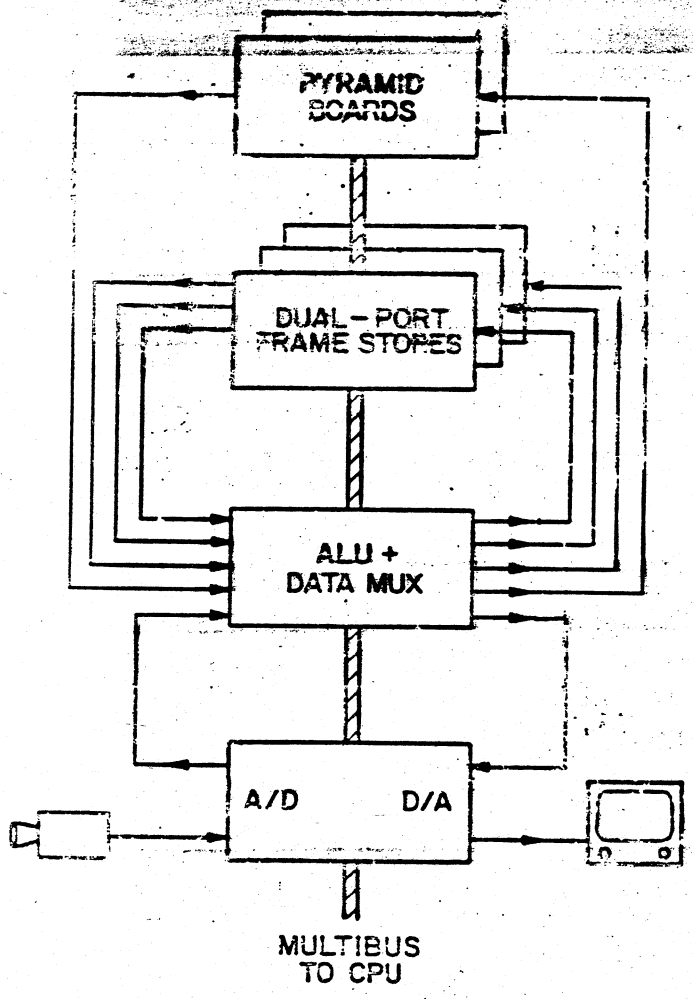


ARRAY SISTOLICI E A FRONTE D'ONDA

WAP

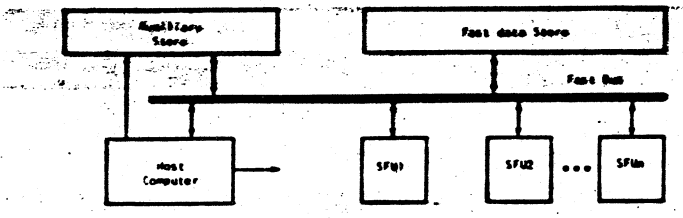


THE PVH SYSTEM



HARDWARE ORIENTED ARCHITECTURES

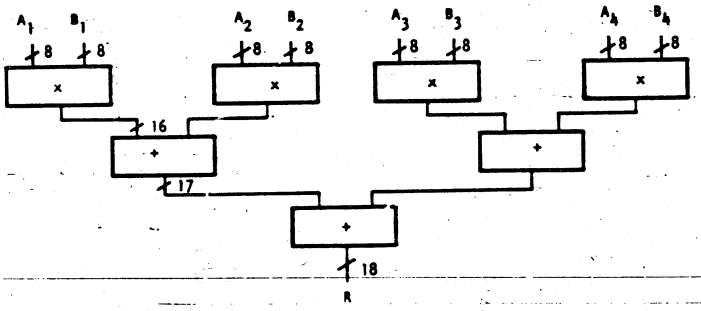
SPECIAL FUNCTION SYSTEMS



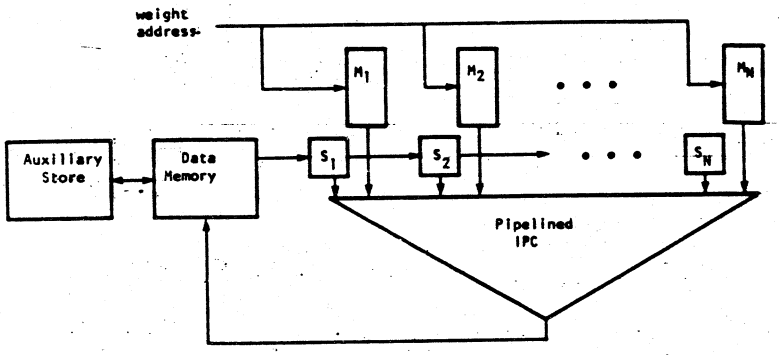
Special Function Processor System

INNER PRODUCT COMPUTERS

$$R = \sum_{i=1}^{n} A_i B_i$$



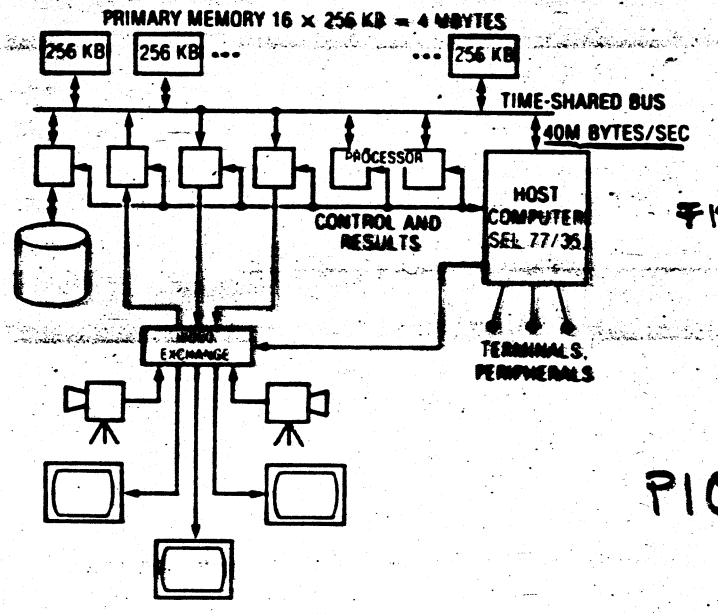
An Inner Product Computer Design.



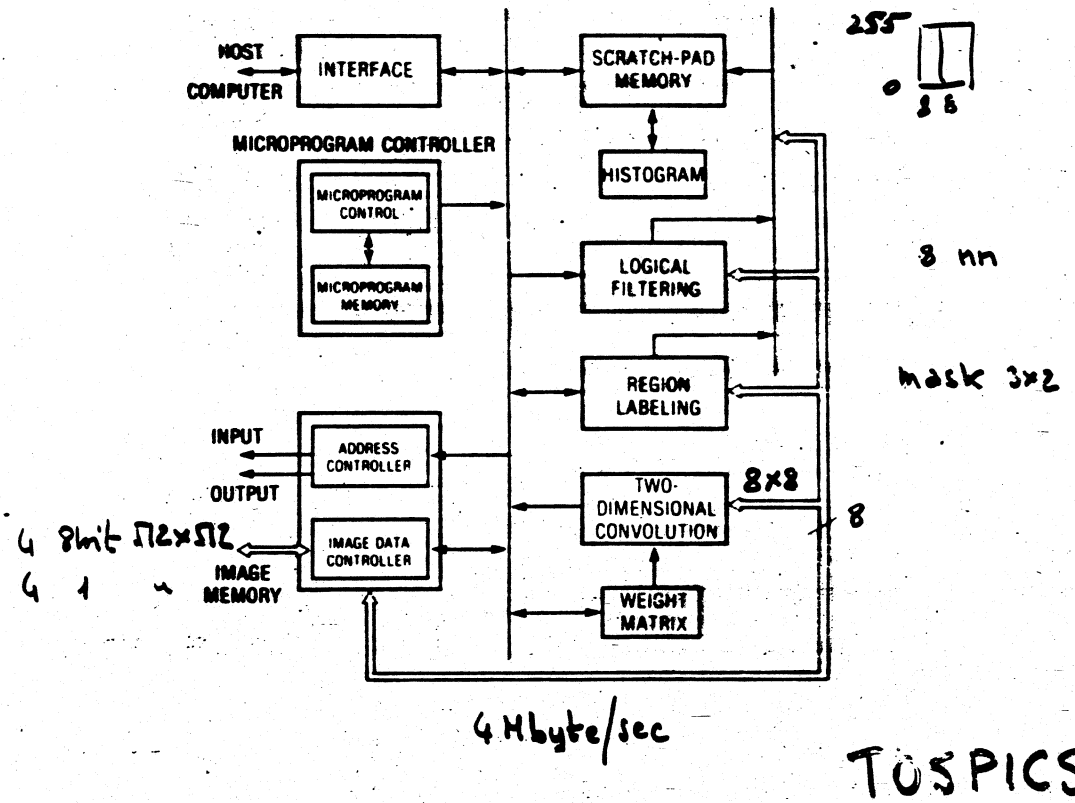
An IPC computer organization for Image Processing.

INTERPROCESSOR COMMUNICATION MODES

HETEROGENEOUS FUNCTIONALLY DEDICATED / BUS ORIENTED STRUCTURES



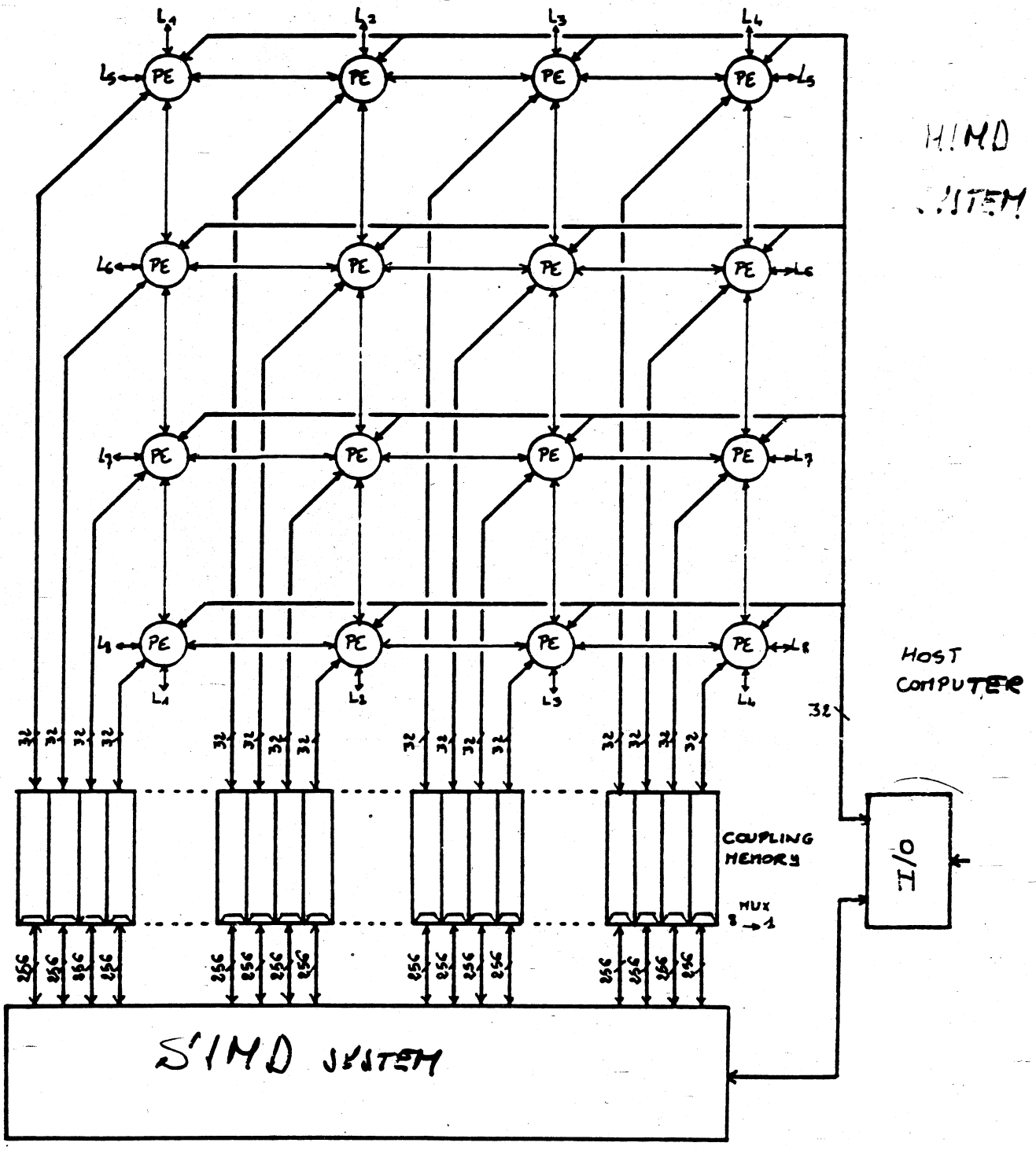
PICAP II



TOSPICS

HIERARCHICAL IP ARCHITECTURE

HETEROGENEOUS / LOOSELY DISTRIBUTED

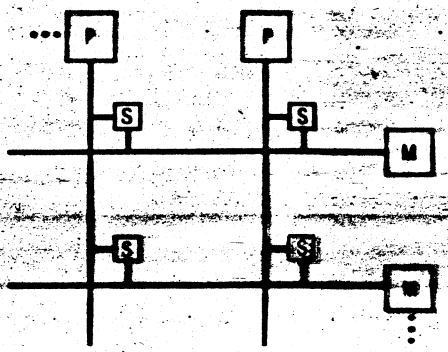


DYNAMIC PERMUTATION STRUCTURES

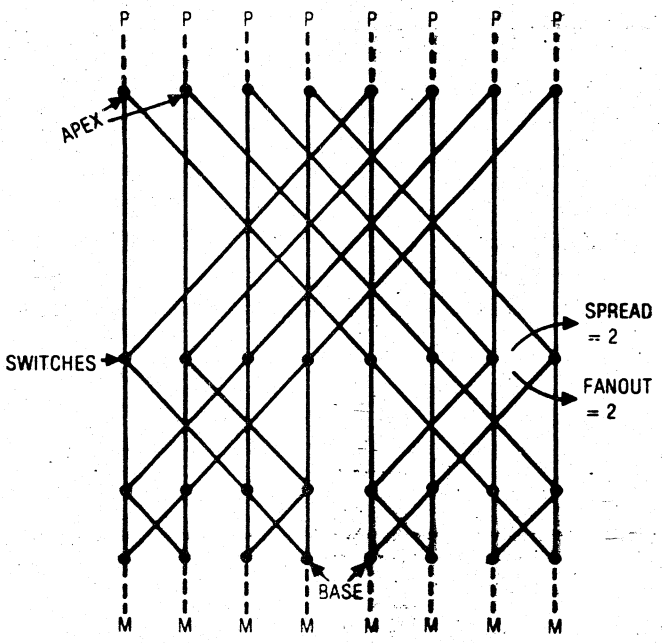
CROSS BAR

N^2 SWITCHING ELEMENTS

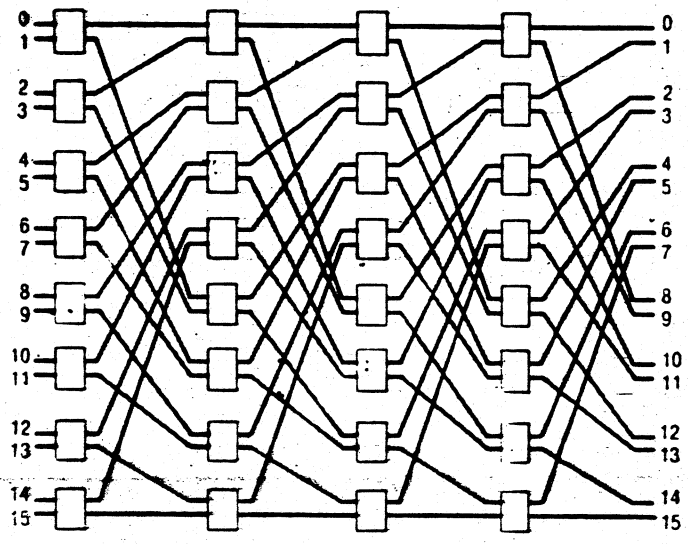
DELAY : 1 LEVEL OF SWITCHING



BANYAN



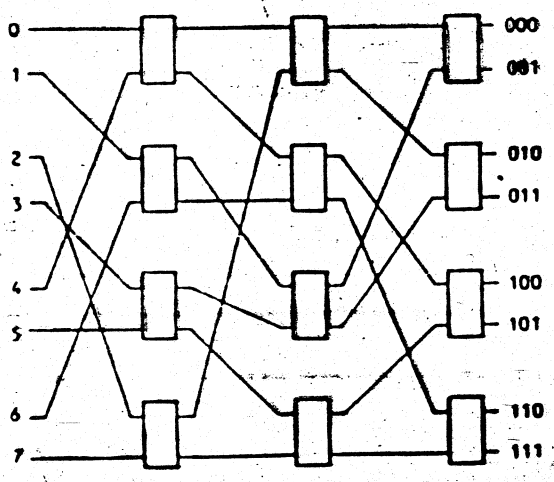
OMEGA

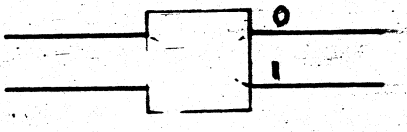


$\frac{N}{2} \log_2 N$ SWITCHING ELEMENTS

DELAY : $\log_2 N$ LEVELS OF SWITCHING

DELTA



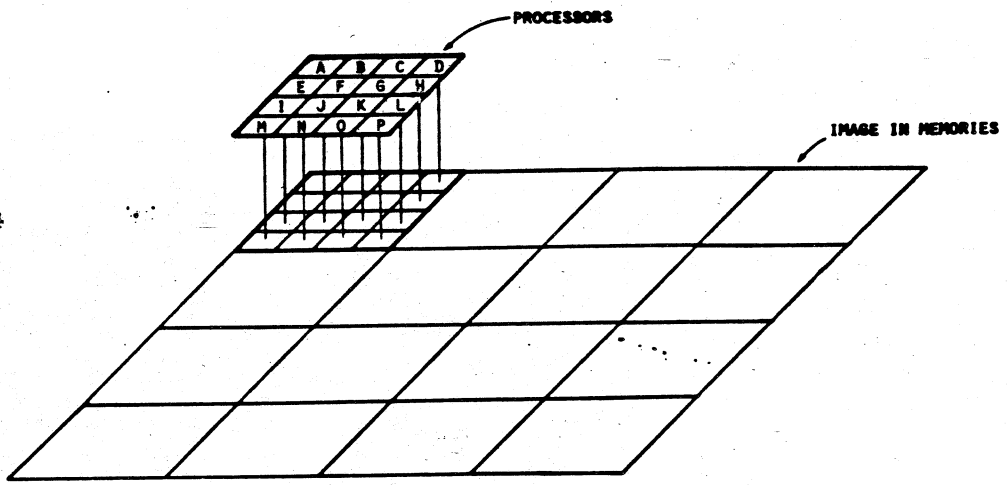


ARRAY OF PROCESSORS

IMAGE ÷ PROCESSORS DISTRIBUTION

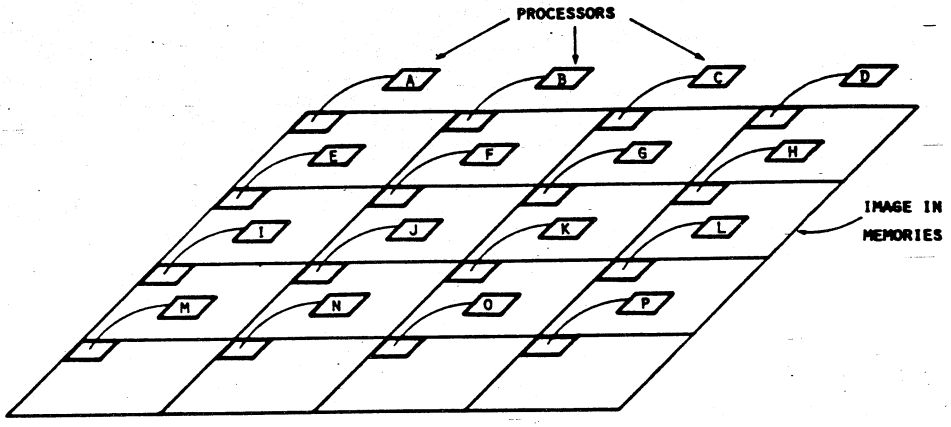
IMAGE DISTRIBUTED OVER THE PEs

HPP, CLIP IV, BASE, GAPP, etc



PEs DISTRIBUTED OVER THE IMAGE

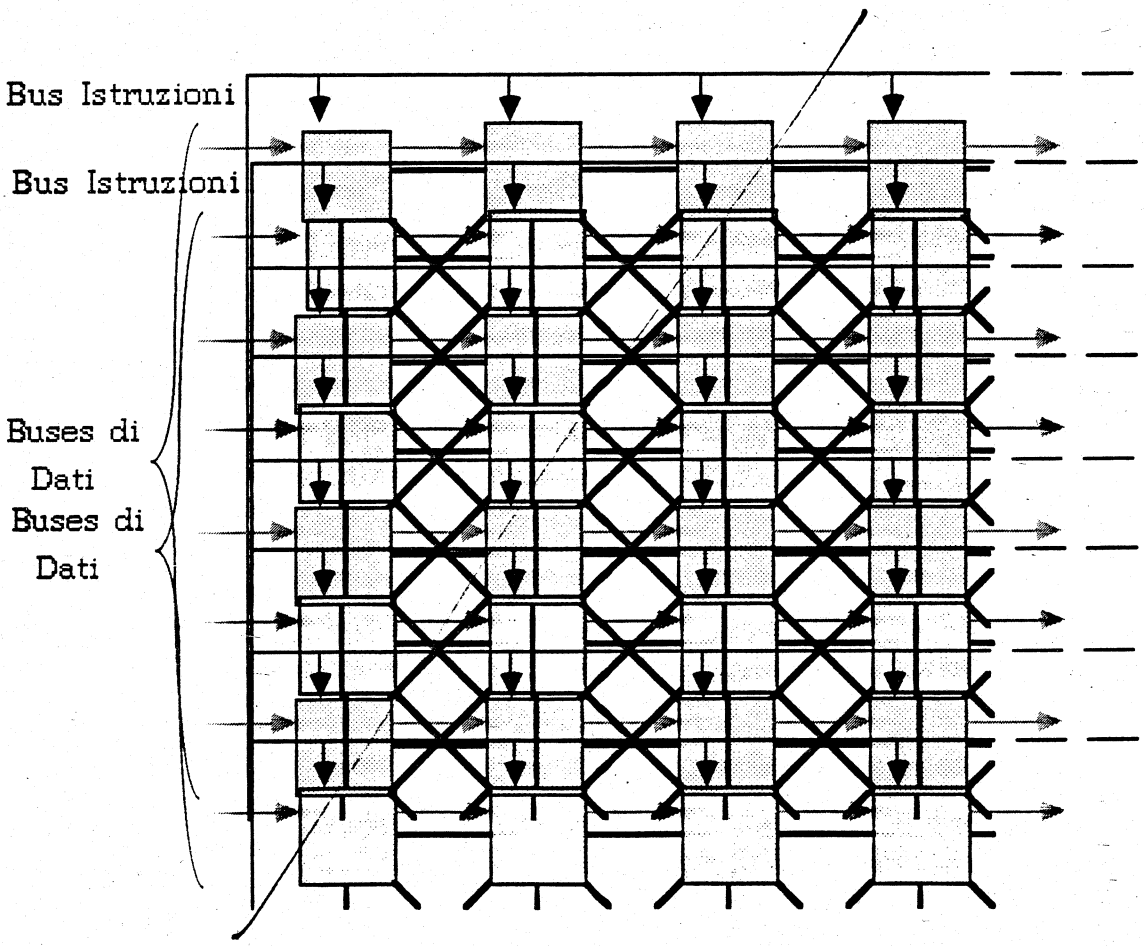
PHP II, LIPP, DAP, etc



IT ARCHITECTURES

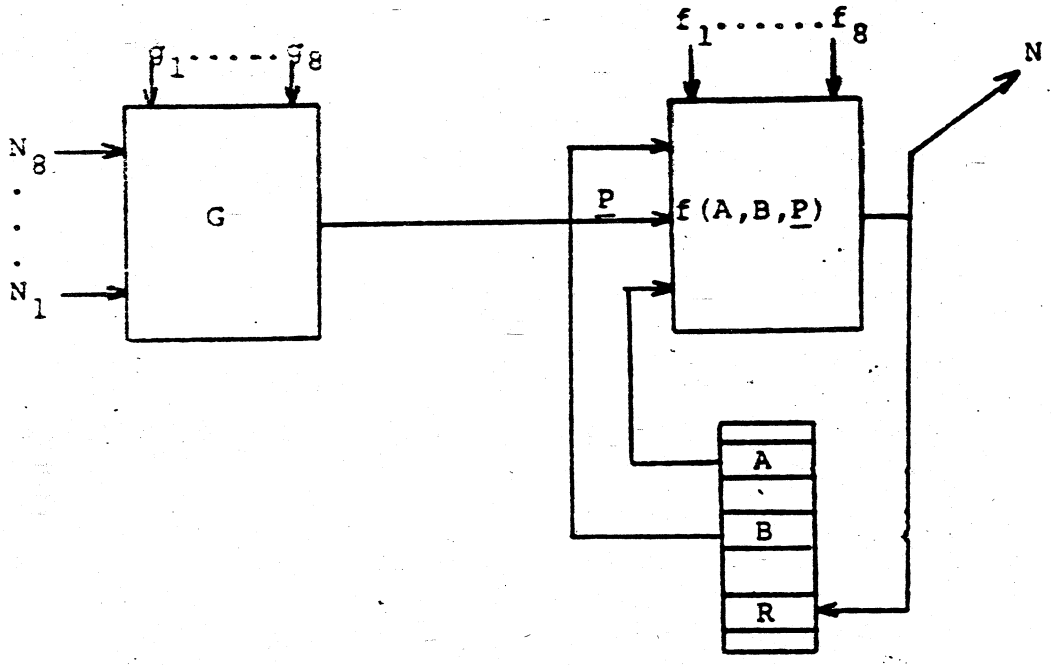
MACCHINA SIMD A GRANA FINE

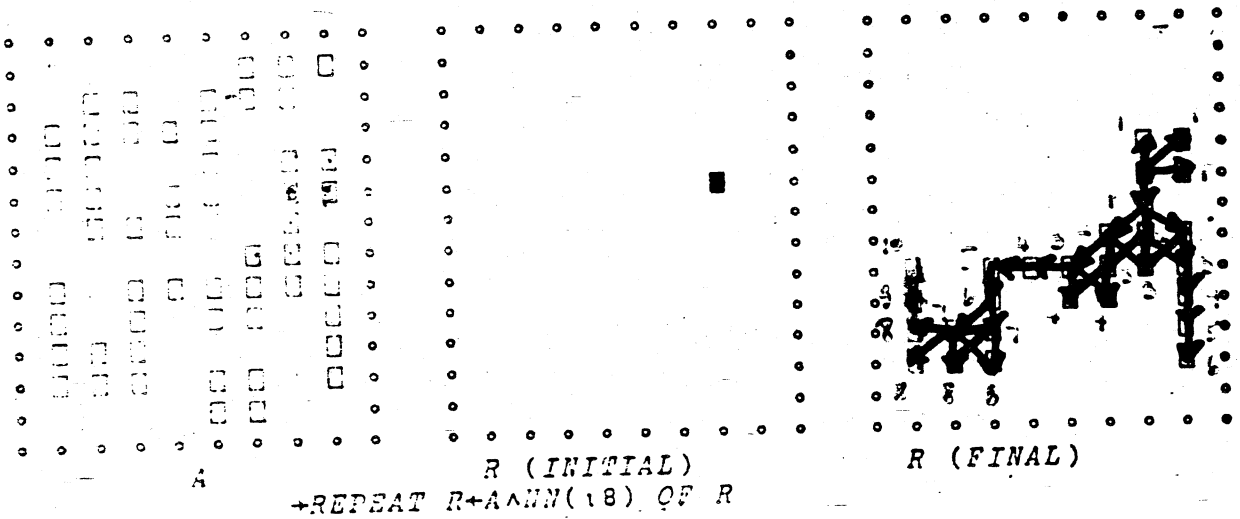
CONNETTIVITA' & BROADCASTING/GATING



SIMD ARRAYS

RECURSIVE NEAR NEIGHBOR INSTRUCTIONS





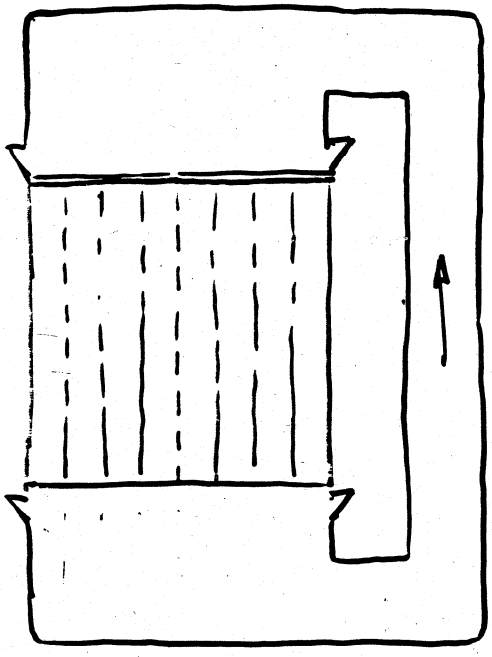
HISTOGRAMMING

I STEP - RAMP GENERATION OR LOADING

1	1	1	1	1	1
2	2	2	2	2	
3	3	3	3	3	
4	4	4	4	4	
5	5	5	5	5	

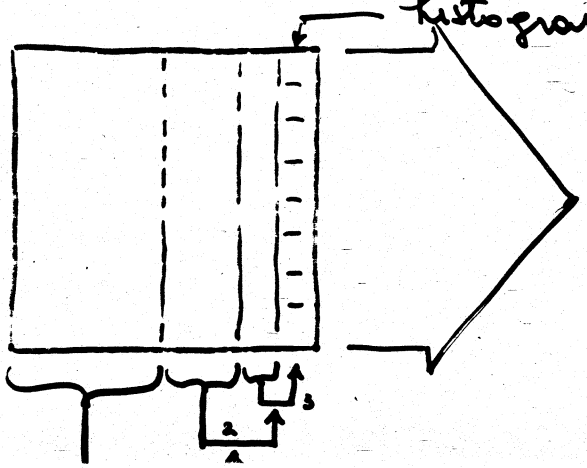
1 (loading)

II STEP - COLUMN HISTOGRAMMING : # CO-OCCURRENCES



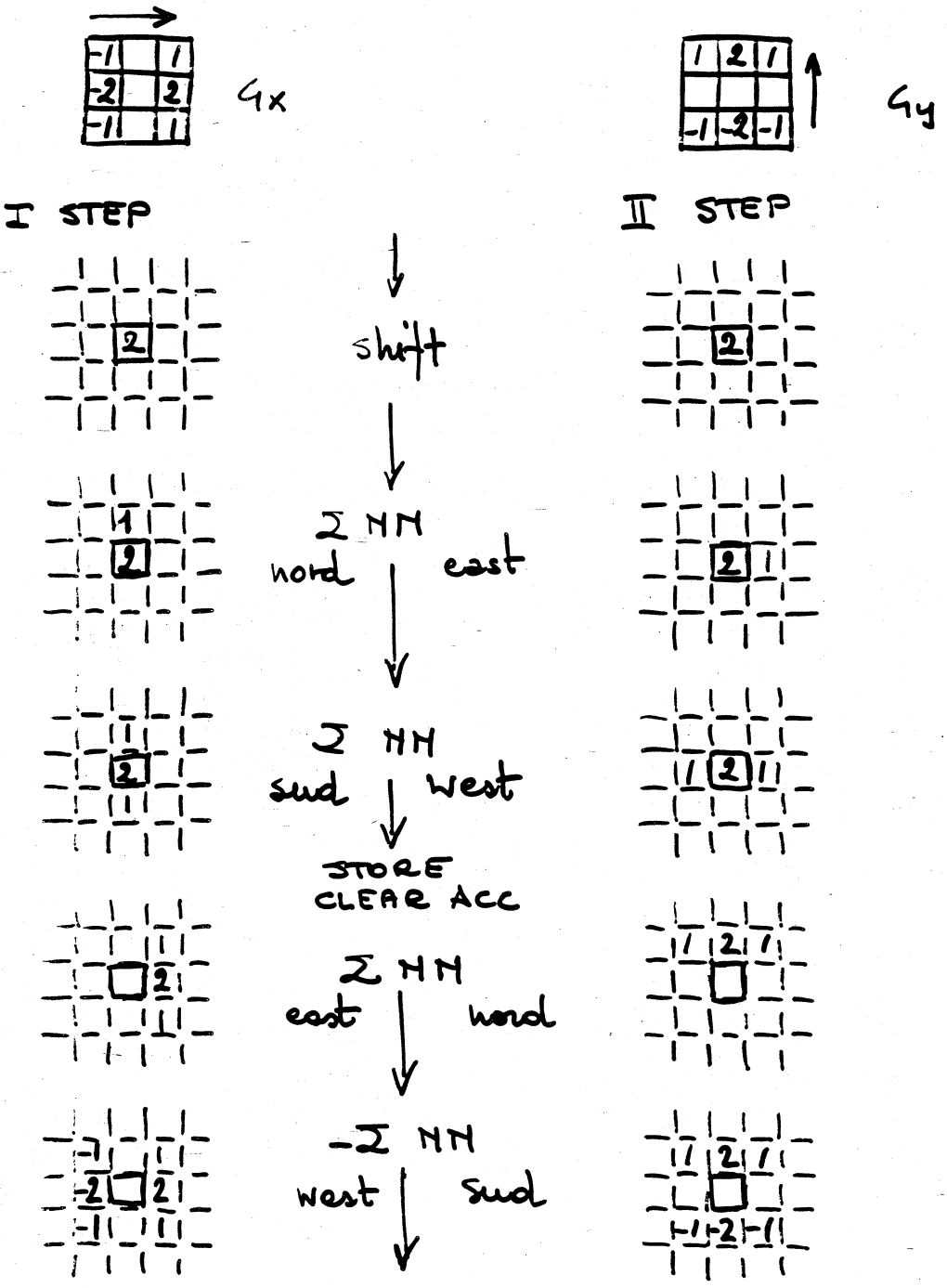
128 shift & compare + increment

III STEP - RECURSIVE DOUBLING



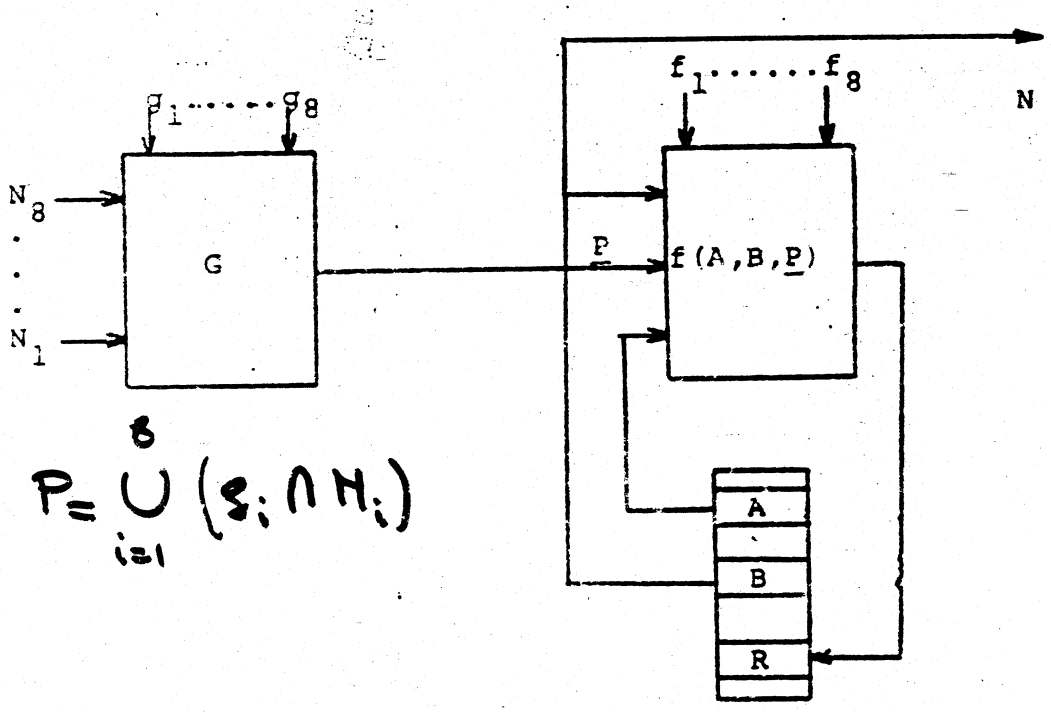
127 shifts & 7 sums

SOBEL'S EDGE DETECTOR OPERATOR

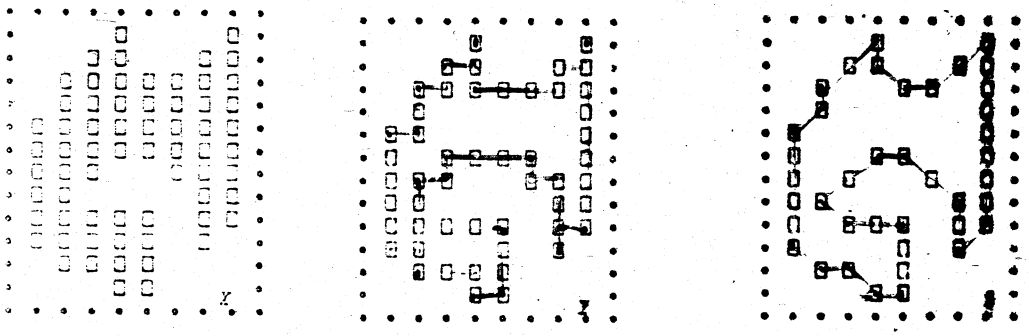


SIMD ARRAYS

SIMPLE LOCAL NEIGH... INSTRUCTIONS



$$P = \bigcup_{i=1}^{8} (g_i \cap N_i)$$



4-Connected Edge Detection

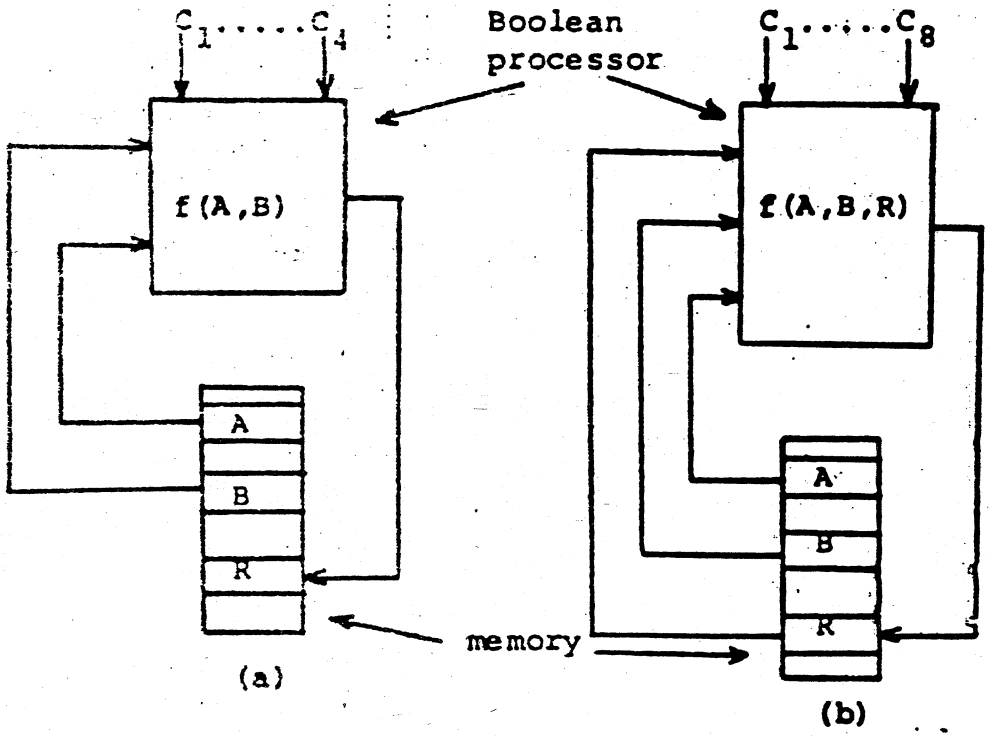
Y ← Y ∧ NN (ALL8) OF ~ X EDGE 1

8-Connected Edge Detection

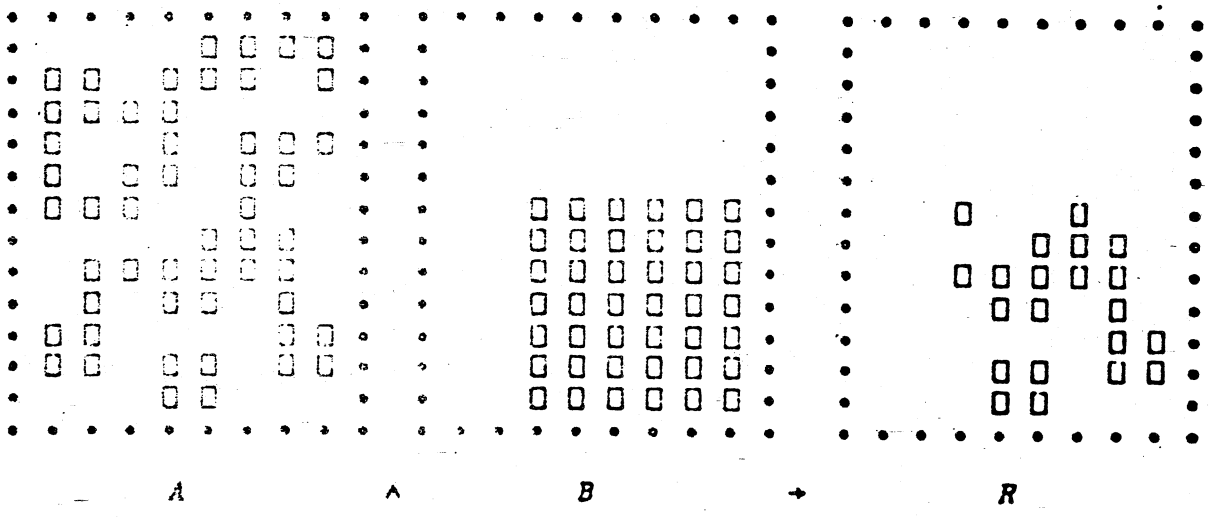
Z ← X ∧ NN (2 4 6 8) OF ~ X EDGE 1

SIMD ARRAYS

BOOLEAN INSTRUCTIONS



Structures for Boolean instruction sub-processors

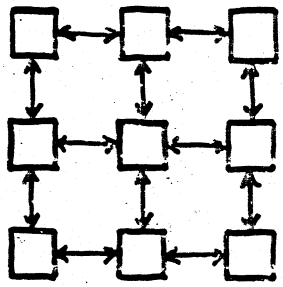


(c)

CELLULAR ARRAYS

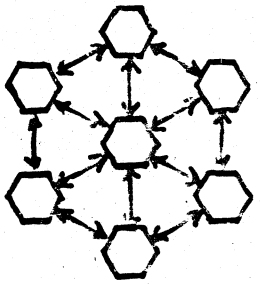
PLANE TESSELLETION

THE NEIGHBORHOOD ACCESS PROBLEM IS THE VON NEUMANN BOTTLENECK OF IMAGE PROCESSING



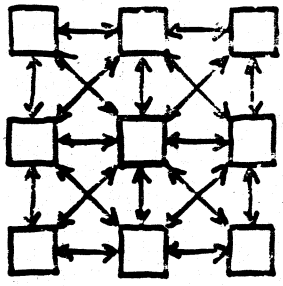
FOUR CONNECTED SQUARE ARRAY

MPP, LIPP, 4APP



SIX CONNECTED HEXAGONAL ARRAY

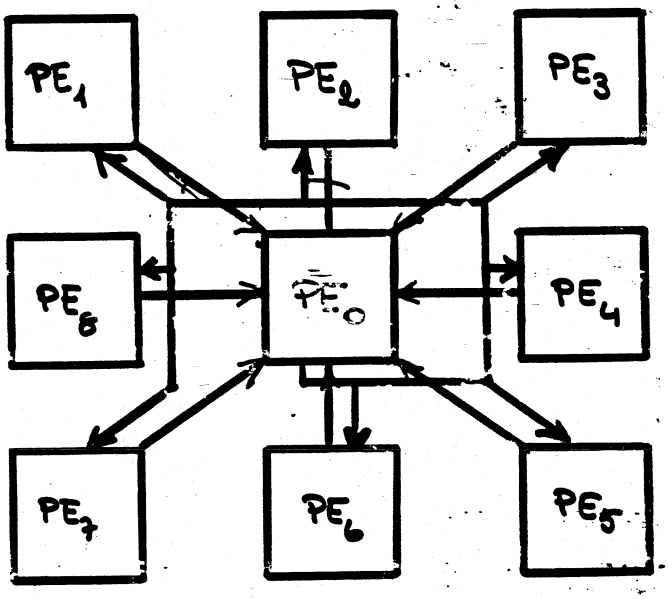
GLOPR., diff 3,



EIGHT CONNECTED SQUARE ARRAY

CLIP IV, PICAP I, Cytocomputer, BASE, PHP

MATRICI DI PROCESSORI



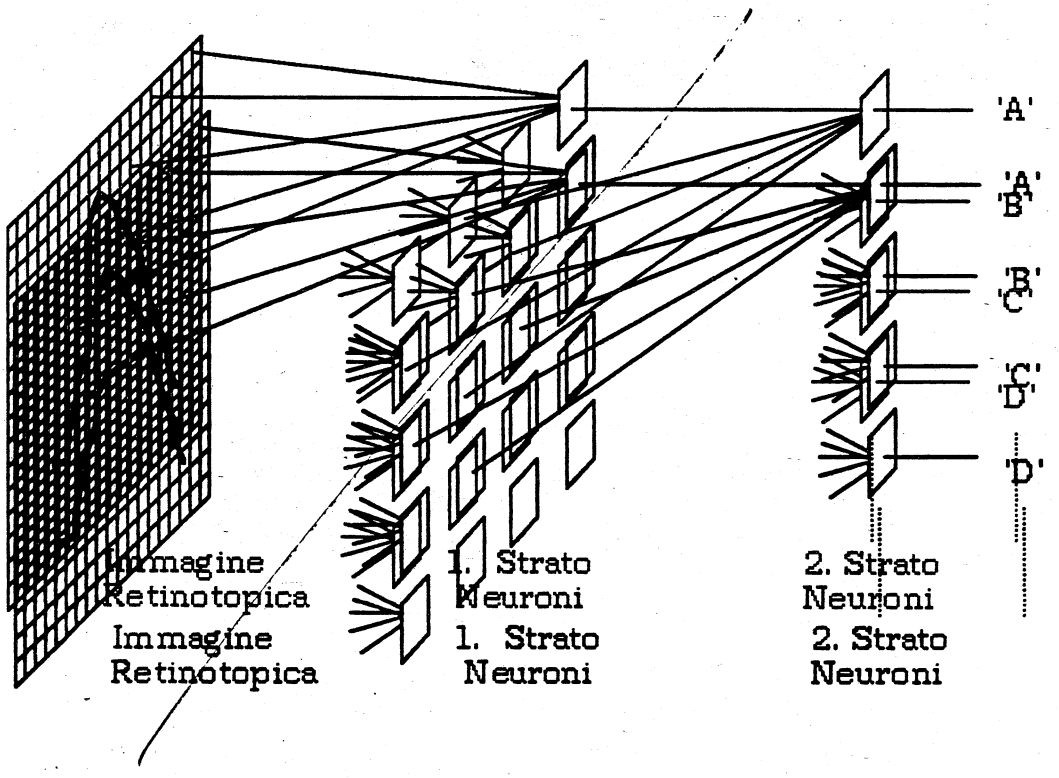
CANALI DEI DATI TRA PROCESSORI ADIACENTI

FINED-GRAINED SIMD SYSTEMS

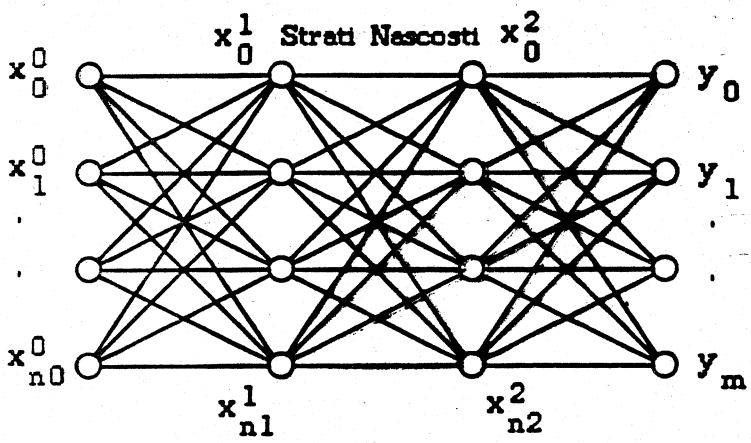
PROCESSOR	SINGLE BIT ALU LOGIC FULL ADD TWO OUTPUT SHIFT REGISTER b) ACTIVITY BIT
ARRAY	BROADCAST INSTRUCTIONS 4-8-? CONNECTIVITY ENABLED INTERCONNECTIONS
STORAGE	LOCAL MEMORY PARALLEL FETCH
LOADING/UNLOADING	ROW SHIFT REGISTER COLUMN PARALLEL ?
CONTROL	DEDICATED EXTERNAL CONTROLLER HOST COMPUTER

RETI NEURALI

PERCEPTRON

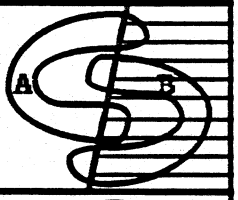
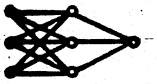
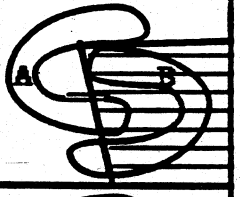


RETI NEURALI MULTISTRATO



$$x_i^s = f\left(\sum_{j=1}^{n_{s-1}} w_{ij}^s x_j^{s-1} - \vartheta_i^s\right)$$

$$0 \le i \le n_s$$

Struttura	Tipo di Regione Discriminante	Esempio di Regione Discriminante
Uno Strato 	Iperpiano	
Due Strati 	Poliedro Convesso	
Tre Strati 	Poliedro Arbitrario